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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/877,027	06/11/2001	Yasuhiko Tsukikawa	57454-138	9823	
7	590 06/05/2002				
McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096			EXAMINER		
			NGUYEN, LINH M		
			ART UNIT	PAPER NUMBER	
			2816		
			DATE MAILED: 06/05/2002		

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. Op/877.027 TSUKIKAWA, YASUHIKO	<u> </u>								
Examiner	•		Application No.	Applicant(s)					
Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE of this communication appears on the cover sheet with the correspondence address = Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE of THIS COMMUNICATION. The MAILING DATE of THIS COMMUNICATION. If the period for reby specified above is less than thiny (30) days, a reply with the statisticy minimum of theiry (30) days will be considered limely. If the period for reby specified above is less than thiny (30) days, a reply with the statisticy minimum of theiry (30) days will be considered limely. If the period for reby specified above is less than thiny (30) days, a reply with the statisticy minimum of theiry (30) days will be considered limely. If the period for reby specified above is less than thiny (30) days, a reply with the statisticy minimum of theiry (30) days will be considered limely. If the period for reby specified above is less than thiny (30) days, a reply with the days of the communication. If the period for reby specified above is less than thiny (30) days and will apply a will a great a retail gate of this communication. If the period for reby specified above is less than thiny (30) days will be considered limely. If the period for reby specified above is less than thiny (30) days will be considered limely. If this period the days are deviced and the statistic principles and the second of the communication. If the period for reby specified and the statistic principles and the second of the second of the mailing date of this communication. If a proved, communication is objected to by the Examiner. Application Papers If a proposed drawing correction filed on is a proved by the Examiner. Application Papers If a proposed drawing correction filed on is a proved by the Examiner. If a proposed drawing correction filed on is a proved to do the priority documents have been received. If the proposed dra			09/877,027	TSUKIKAWA, YASUHI	ко				
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THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.13(g), in no event, however, may a reply be sinely field able 19X (9) MONTHS from the mailing date of this communication of 19X (9) MONTHS from the mailing date of this communication. ### SECTION OF THE COMMUNICATION OF THE COMMUNICAT	Period fe	The MAILING DATE of this communication app or Reply	pears on the cover sheet	with the correspondence address	s				
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DETAILED ACTION

This is a reply to the Applicant's amendment submitted on April 19th, 2002, according to which claims 1-17 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1, 4, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (U.S. Patent No. 5,805,003).

With respect to claims 1 and 4, Hsu discloses, in figure 3, a synthesizing apparatus using a delay locked loop circuit comprising (1) an input buffer [12] for receiving an external clock [Fin] and outputting a first clock signal [20], (2) a delay circuit [22, 24, 26, 28] for delaying a first clock signal [20] and outputting a second clock signal [32], (3) a detector [37] for detecting a phase difference between the first and second internal clocks, and (4) a gray code counter [16] using a gray code and being responsive to an output of the detector for generating a signal [54] and adjusting an amount of delay of the delay circuit.

With respect to claim 14, figure 3 of Hsu shows a corresponding control method which comprises the steps of (1) inputting an external clock [Fin] to an input buffer [12] to generate a first internal clock [20] therefrom, (2) delaying the first internal clock [20] to output a second internal clock, (3) detecting a phase difference between the first and second internal clocks, and

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(4) using a gray code to determine an amount of delay to be applied in the step of delaying, wherein the amount of delay corresponds to a result obtained in the step of detecting.

Allowable Subject Matter

- 3. Claims 11-13 are allowed.
- 4. Claims 2-3, 5-10, and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art of record does not show or fairly suggest 1) a gray code counter including a) a gray code register storing said gray code; b) a binary code converter converting said gray code into a binary code; c) an upward carry/downward carry generator using said binary code stored in said binary code converter, to generate an upward carry signal and a downward carry signal; and d) a carry multiplexer generating from said upward carry signal and said downward carry signal a carry signal corresponding to a result obtained by said detector, for updating said gray code in said gray code register, as called for in claims 2, 5, and the corresponding method claim 15, and 2) a delay locked loop including a combination of a) a first input buffer receiving at least a first external clock and a second external clock complementary in phase to the first external clock, and outputting a first internal clock at the timing of the rising edge of the first external clock when a potential of the first external clock is equal to that of the second external clock when a potential clock at the timing of the rising edge of the second external clock when a potential of the first external clock is equal to that of the second external clock when a potential of the first external clock is equal to that of the second external clock when a

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circuit delaying the first internal clock to output a third internal clock; d) a second delay circuit delaying said second internal clock to output a fourth internal clock; e) a detector detecting a phase difference between the first and third internal clocks; and f) a gray code counter using a gray code, responsive to an output of the detector for generating a signal adjusting an amount of delay of the first delay circuit and an amount of delay of the second delay circuit, as called for in claim 11.

Remarks and conclusion

5. The Applicant's arguments on the cited prior art have been acknowledged. However, the limitations claimed in claims 1, 4, and 14 can not overcome the teachings of a newly found prior art to Hsu (U.S. Patent No. 5,805,003); therefore, claims 1, 4, and 14 are anticipatory rejected by Hsu.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen

TIME THY P. CALLAHAN
PERMISORY PATENT EXAMINER

TECHNOLOGY CENTER 2800